In The Claims:

1. A method to allow repeatable system behavior in an integrated circuit having multiple clock domains created by a plurality of synchronous clocks comprising:

creating a global framing clock that is synchronized with the plurality of synchronous clocks and that has a rising or falling edge that corresponds to the rising or falling edges of the plurality of synchronous clocks; and

using the global framing clock to control a chip function.

2. The method of claim 1, wherein the global framing clock has a frequency equal to the lowest common denominator of the speeds of the plurality of synchronous clocks or to some divisor thereof and wherein the global framing clock is used to control the plurality of synchronous clocks.

3. The method of claim 1, wherein the global framing clock is used to control the issuance of an asynchronous event to the chip.

4. The method of claim 3, further comprising:

receiving the asynchronous event;

waiting for a rising edge of the global framing clock; and

releasing the asynchronous event to the system when the rising edge of the global framing clock occurs.

5. The method of claim 4, wherein the asynchronous event is a reset signal.

6. The method of claim 4, further comprising connecting the global framing clock to a system having a plurality of integrated circuits to create a common reference clock in the plurality of integrated circuits.

7. The method of claim 4, further comprising:

using the global framing clock as an input into a flip-flop;

using a system clock as a clock for the flip-flop;

receiving a framing clock data stream as an output from the flip-flop; and

using the framing clock data stream to control the issuance of the asynchronous event.

8. A computer system having multiple clock domains comprising:

a system clock;

at least one intermediate clock that is synchronized with the system clock and has a slower frequency than the system clock;

a global framing clock; and

an integrated circuit that receives the global framing clock, the system clock, and the at least one intermediate clock;

wherein the global framing clock controls a function of the integrated circuit.

9. The computer system of claim 8, wherein the global framing clock has a rising edge that corresponds to the rising edges of the system clock and of the at least one intermediate clock.

10. The computer system of claim 9, wherein the global framing clock has a frequency equal to the lowest common denominator of the frequencies of the system clock and the at least one intermediate clock, or to some divisor thereof.

11. The computer system of claim 8, wherein the global framing clock controls a function of the system.

12. The computer system of claim 11, wherein the global framing clock controls the issuance of an asynchronous event to the system.

13. The computer system of claim 12, wherein the asynchronous event is a system reset function.

14. The computer system of claim 12, further comprising a flip-flop that receives the global framing clock as an input and outputs a framing clock data stream, which data stream may be used to control the asynchronous event.

15. A method of creating repeatability of a system having multiple clock domains created by a plurality of intermediate clocks by causing a system reset function to take effect in all clock domains at the same time comprising:

creating a global framing clock having a rising edge that corresponds to the rising edges of the plurality of clocks;

receiving an asynchronous event;

waiting for a rising edge of the global framing clock; and

releasing the asynchronous event to the system when the rising edge of the global framing clock occurs.

16. The method of claim 15, wherein the asynchronous event is a system reset signal.

17. The method of claim 16, wherein the global framing clock has a frequency equal to the lowest common denominator of the plurality of intermediate clocks or to some divisor thereof.

18. The method of claim 17, further comprising:

receiving a system clock into a clock divider;

dividing the system clock into the global framing clock using the clock divider;

receiving the global framing clock into a flip-flop timed by the system clock; and

using a output data stream from the flip-flop as a framing clock to control the release of the system reset signal to the system.

19. The method of claim 18, further comprising:

detecting an edge of the framing clock; and

releasing the reset signal to the system when the edge of the framing clock is detected.